Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Please amend Claims 3, 19, 23, and 28, as follows.

Claim 1 (canceled)

Claim 2 (previously presented): The method of claim 3, wherein the rise time generic variable comprises the rise time delay value copied from the tuple, and wherein the fall time generic variable comprises the fall time delay value copied from the tuple.

Claim 3 (currently amended): A method <u>for delay correlation analysis for VHDL modeling,</u> comprising:

copying a rise time delay value and a fall time delay value from a tuple of a VHDL generic variable;

storing a rise time generic variable and a fall time generic variable, the rise time generic variable comprising at least one rise time delay value and the fall time generic variable comprising at least one fall time delay value;

storing the at least one rise time delay value and the at least one fall time delay value according to a predetermined correlation policy;

removing at least one duplicate rise time delay value from the at least one rise time delay value; and

removing at least one duplicate fall time delay value from the at least one fall time delay value.

Claim 4 (original): The method of claim 3, wherein the correlation policy represents a correlation of occurrences of delay values in a VHDL standard delay file.

Claim 5(original): The method of claim 3, wherein method further comprises:

grouping, into at least one correlation set, one of

the at least one rise time delay value into a rise time delay correlation set; and

the at least one fall time delay value into a fall time delay correlation set.

Claim 6 (original): The method of claim 3, wherein method further comprises:

sorting at least one set of

the at least one rise time delay value; and

the at least one fall time delay value.

Claim 7 (original): The method of claim 3, further comprising:

collecting generic variables from a VHDL standard delay file;

selecting a generic variable; and

extracting delay values for the selected generic variable.

Claim 8 (original): The method of claim 3, further comprising:

grouping delay values into correlation sets, wherein each of the correlation sets comprises a group of delay values up to a predetermined maximum number of delay values.

Claim 9(original): The method of claim 8, wherein the predetermined maximum number of delay values in a group is 256.

Claim 10 (original): The method of claim 3, wherein method further comprises:

outputting an analysis file based on the at least one rise time delay value and the at least one fall time delay value.

Claim 11 (original): The method of claim 10, wherein the analysis file comprises a data structure comprising:

a first field containing an ISO 8859-1 character representing an index position in a correlation set; and

a set of fields, each field containing an ISO 8859-1 character representing a delay value position of a delay name in a VHDL logic gate model.

Claim 12 (original): The method of claim 10, wherein the analysis file comprises a data structure comprising:

a set of fields, each field containing an ISO 8859-1 character indexing a set of slots containing positions for delay values of a delay name in a VHDL logic gate model; and

a second set of fields, each field containing an ISO 8859-1 character indexing the position of the delay value within the indexed slot.

Claim 13 (original): The method of claim 10, wherein the analysis file comprises a data structure comprising:

a set of fields, each field containing an ISO 8859-1 character representing a first digit of a delay value of a delay name in a VHDL logic gate model;

a second set of fields, each field containing an ISO 8859-1 character representing a second digit of a delay value of a delay name in a VHDL logic gate model; and

a third set of fields, each field containing an ISO 8859-1 character representing a third digit of a delay value of a delay name in a VHDL logic gate model.

Claim 14 (original): The method of claim 13, wherein each delay value is evaluated as the sum of a 3-digit number and a predetermined offset value.

Claim 15 (original): The method of claim 14, wherein the 3-digit number comprises a base 62 number represented by alphanumeric characters.

Claim 16 (original): The method of claim 10, wherein the analysis file comprises a 3-dimensional variable array data structure wherein:

a z-axis of the data structure represents a set of common blocks for each logical topology of a VHDL logic gate;

an x-axis of the data structure represents a delay name for the gate topology; and

a y-axis of the data structure represents an actual delay value.

Claim 17 (original): The method of claim 16, wherein the z-axis of the data structure represents a generic delay name common to a plurality of logic gates.

Claim 18 (original): The method of claim 10, further comprising:

collecting delay values from a VHDL standard delay file according to a second predetermined correlation policy;

sorting the delay values;

removing duplicate delay values;

grouping the delay values into correlation sets;

outputting a second analysis file;

generating statistical data for the analysis file and the second analysis file; and

comparing the statistical data to determine which correlation policy is most efficient.

Claim 19 (currently amended): An apparatus <u>for delay correlation analysis for VHDL modeling</u>, comprising:

a controller/processor;

a data memory, communicatively coupled to the controller/processor, for storing a VHDL standard delay file; and

an SDF analyzer, communicatively coupled to the controller/processor and the data memory, for collecting delay values from the VHDL standard delay file by copying from each VHDL generic variable in the VHDL standard delay file a rise time delay value and a fall time delay value from a tuple of the VHDL generic variable, and for storing in the data memory a rise time generic variable and a fall time generic variable, the rise time generic variable comprising at least one rise time delay value and the fall time generic variable comprising at least one fall time delay value.

Claim 20 (original): The apparatus of claim 19, wherein the SDF analyzer for organizing the rise time generic variable and the fall time generic variable in the data memory according to a predetermined correlation policy.

Claim 21 (original): The apparatus of claim 20, wherein the SDF analyzer for

organizing the rise time generic variable in the data memory by sorting the at least one rise time delay value, removing any duplicate rise time delay value, and grouping the at least one rise time delay value into at least one correlation set, and for

organizing the fall time generic variable in the data memory by sorting the at least one fall time delay value, removing any duplicate fall time delay value, and grouping the at least one fall time delay value into at least one correlation set.

Claim 22 (original): The apparatus of claim 19, wherein the rise time generic variable and the fall time generic variable are stored in an SDF analysis file in the data memory.

Claim 23 (currently amended): A system <u>for delay correlation analysis for VHDL modeling</u>, comprising:

a memory for storing a VHDL standard delay file; and

an SDF analyzer, communicatively coupled to the memory, for copying from each VHDL generic variable in the VHDL standard delay file a rise time delay value and a fall time delay value from a tuple of the VHDL generic variable, and for storing in the memory a rise time generic variable and a fall time generic variable, the rise time generic variable comprising at least one rise time delay value and the fall time generic variable comprising at least one fall time delay value, the at least one rise time delay value including the rise time delay value copied from the tuple of the VHDL generic variable in the VHDL standard delay file, and the at least one fall time delay value including the fall time delay value copied from the tuple of the VHDL generic variable in the VHDL standard delay file.

Claim 24 (original): The system of claim 23, wherein the at least one rise time delay value being sorted, with any duplicate rise time delay value being removed, and organized according to a predetermined correlation policy, and wherein the at least one fall time delay value being sorted, with any duplicate fall time delay value being removed, and organized according to a predetermined correlation policy.

Claim 25 (original): The system of claim 24, wherein the rise time generic variable and the fall time generic variable are stored in memory in an SDF analysis file.

Claim 26 (canceled)

Claim 27 (previously presented): The computer readable medium of claim 28, wherein the rise time generic variable comprises the rise time delay value copied from the tuple, and wherein the fall time generic variable comprises the fall time delay value copied from the tuple.

Claim 28 (currently amended): A computer readable medium comprising computer instructions for <u>delay correlation analysis for VHDL modeling by</u>:

copying a rise time delay value and a fall time delay value from a tuple of a VHDL generic variable;

storing a rise time generic variable and a fall time generic variable, the rise time generic variable comprising at least one rise time delay value and the fall time generic variable comprising at least one fall time delay value; and

storing the at least one rise time delay value and the at least one fall time delay value according to a predetermined correlation policy;

removing at least one duplicate rise time delay value from the at least one rise time delay value; and

removing at least one duplicate fall time delay value from the at least one fall time delay value.

Claim 29 (original): The computer readable medium of claim 28, wherein the correlation policy represents a correlation of occurrences of delay values in a VHDL standard delay file.

Claim 30 (original): The computer readable medium of claim 28, further comprising computer instructions for:

grouping, into at least one correlation set, one of

the at least one rise time delay value into a rise time delay correlation set;

and

the at least one fall time delay value into a fall time delay correlation set.

Claim 31 (original): The computer readable medium of claim 28, further comprising computer instructions for:

sorting at least one set of

the at least one rise time delay value; and

the at least one fall time delay value.

Claim 32 (original): The computer readable medium of claim 28, further comprising computer instructions for:

collecting generic variables from a VHDL standard delay file;

selecting a generic variable; and

extracting delay values for the selected generic variable.

Claim 33 (original): The computer readable medium of claim 28, further comprising computer instructions for:

grouping delay values into correlation sets, wherein each of the correlation sets comprises a group of delay values up to a predetermined maximum number of delay values.

Claim 34 (original): The computer readable medium of claim 33, wherein the predetermined maximum number of delay values in a group is 256.

Claim 35 (original): The computer readable medium of claim 28, further comprising computer instructions for:

outputting an analysis file based on the at least one rise time delay value and the at least one fall time delay value.

Claim 36 (original): The computer readable medium of claim 35, wherein the analysis file comprises a data structure comprising:

a first field containing an ISO 8859-1 character representing an index position in a correlation set; and

a set of fields, each field containing an ISO 8859-1 character representing a delay value position of a delay name in a VHDL logic gate model.

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Claim 37 (original): The computer readable medium of claim 35, wherein the analysis file comprises a data structure comprising:

a set of fields, each field containing an ISO 8859-1 character indexing a set of slots containing positions for delay values of a delay name in a VHDL logic gate model; and

a second set of fields, each field containing an ISO 8859-1 character indexing the position of the delay value within the indexed slot.

Claim 38 (original): The computer readable medium of claim 35, wherein the analysis file comprises a data structure comprising:

a set of fields, each field containing an ISO 8859-1 character representing a first digit of a delay value of a delay name in a VHDL logic gate model;

a second set of fields, each field containing an ISO 8859-1 character representing a second digit of a delay value of a delay name in a VHDL logic gate model; and

a third set of fields, each field containing an ISO 8859-1 character representing a third digit of a delay value of a delay name in a VHDL logic gate model.

Claim 39 (original): The computer readable medium of claim 38, wherein each delay value is evaluated as the sum of a 3-digit number and a predetermined offset value.

Claim 40 (original): The computer readable medium of claim 39, wherein the 3-digit number comprises a base 62 number represented by alphanumeric characters.

Claim 41 (original): The computer readable medium of claim 35, wherein the analysis file comprises a 3-dimensional variable array data structure wherein:

a z-axis of the data structure represents a set of common blocks for each logical topology of a VHDL logic gate;

an x-axis of the data structure represents a delay name for the gate topology; and

a y-axis of the data structure represents an actual delay value.

Claim 42 (original): The computer readable medium of claim 41, wherein the z-axis of the data structure represents a generic delay name common to a plurality of logic gates.

Claim 43 (original): The computer readable medium of claim 35, further comprising instructions for:

collecting delay values from a VHDL standard delay file according to a second predetermined correlation policy;

sorting the delay values;

removing duplicate delay values;

grouping the delay values into correlation sets;

outputting a second analysis file;

generating statistical data for the analysis file and the second analysis file; and

comparing the statistical data to determine which correlation policy is most efficient.